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Modeling and Reliability of NanoSatellites Attitude Determination and Control System (ADCS)

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Modeling and Reliability of NanoSatellites Attitude Determination and Control System (ADCS)

Abstract: Nanosatellites must be oriented, in their orbits, around their center of mass. Their antennas and their sensors must be pointed at a specific area of the Earth. Their attitudes controls must take into account different disturbances, external and internal, acting on the system and affecting its orbit and its attitude or both. To ensure the success and the safety of a nanosatellite mission, an on-board (Attitude Determination and Control System) ADCS is required. This very complex system is crucial to control the attitude. This ADCS cannot be optimized without the modeling of the system or its attitude. In this work, an Attitude representation block used to model the Attitude of a Nanosatellite is presented.

Reliability is an important design constraint for critical applications at ground-level and aerospace. SRAM-based FPGAs are attractive for critical applications due to their high performance and flexibility. However, they are susceptible to radiation effects such as soft errors in the configuration memory. Moreover, the effects of voltage scaling and aging increment the sensitivity of SRAM-based FPGAs to soft errors. Experimental results in the literature show that voltage scaling and aging can increase at least two times the susceptibility of SRAM-based FPGAs to Soft Error Rate (SER). These findings are innovative because they combine three real effects that occur in SRAM-based FPGAs. Results can guide designers to predict soft error effects during the lifetime of devices operating at different power supply voltages. Memory scrubbing is an effective method to correct soft errors in SRAM memories, nevertheless it imposes an overhead in terms of silicon area and energy consumption. In this thesis, it is proposed a novel scrubbing technique using time redundancy called Cyclic Redundancy Check Readback Scrubbing (CRC Readback scrubbing) with minimum energy consumption and area overhead without compromising the correction capabilities.

As a case study, the CRC Readback scrubbing will be implemented on a mid-size XilinxVirtex- 5 FPGA device, occupying less area of available slices and consumes less energy per scrubbed frame than a classic Readback or Blind scrubber. Also, the technique repair time is reduced by avoiding the use of an external memory called "Golden" memory for reference.

Keywords: Nanosatellites, Attitude control, ADCS, Faults tolerance, Reliability, SRAM based FPGA, Configuration memory, Memory scrubbing, Time redundancy.